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PATENT ABSTRACTS OF JAPAN

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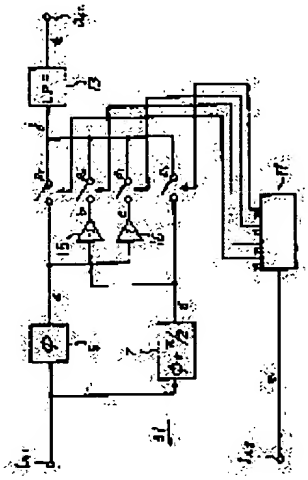
(54) FREQUENCY CONVERSION CIRCUIT

(57)Abstract:
PURPOSE: To eliminate the need for provision of DC balance by applying sets of timing pulse to sets of switches, applying switching control to each switch so as to output a signal whose frequency is converted into a sum or a difference between an input signal frequency and a local oscillating signal frequency from a low pass filter.
CONSTITUTION: A clock signal (e) is fed to a timing pulse generator 11 from an input terminal Iη2 and the timing pulse generator 11 generates an outputs timing pulses T1-T4 and they are fed to switches S1-S4 respectively, which are on/off-controlled. That is, when each of the timing pulses T1-T4 is at an H level, since the switches S1-S4 are closed, signals (j) are synthesized and the resulting signal is fed to an LPF (low pass filter) 13. A high frequency switching component is eliminated in the LPF 13 and a signal (k) is outputted from an output terminal Out. Thus, a problem of DC balance or linearity or the like is not almost caused.



LEGAL STATUS

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